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ART UNIT	PAPER NUMBER
2838	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PTO-PAT-Email@rfem.com

Office Action Summary	Application No.	Applicant(s)	
	10/511,328	THORSOE ET AL.	
	Examiner	Art Unit	
	Alexis Boateng	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *3/16/07*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-10 and 12-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-10 and 12-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 2 – 3, 10 – 12, 15, and 16 - 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Saeki (U.S. 6,051,955).

Regarding claims 16, Saeki discloses wherein a charge control circuit for a battery pack comprising:

rechargeable battery elements (figure 3 items E_{1-2}), which are arranged in respective parallel branches of parallel circuit of battery voltage sources (figure 3 items E_{1-2}; column 4 lines 52 – 55), the charge control circuit comprising state monitoring means for monitoring the battery state of elements (figure 3 item 2; column 5 line 65 – column 6 line 13), and the charge control circuit comprising switches (figure 3 items 5 - 8), which can be controlled by the state monitoring means for interrupting the current flow or releasing the current flow (column 5 line 65 – column 6 line 13), characterized in that each parallel branch has associated state monitoring means and in that respective switch (figure 3 items 5 - 8) is provided in each parallel branch (figure 3 item 2; column 5 line 65 – column 6 line 13), it being possible for said respective switch to be controlled on the basis of

the battery state, which is monitored by the state monitoring means, of the relevant parallel branch in order to selectively block or release only this relevant branch for current flow (column 5 line 65 – column 6 line 13).

Regarding claim 2, Saeki discloses wherein the state monitoring means of a parallel branch are set to switch the controllable switch to the interrupted state when it detects a battery state "parallel branch fully charged" (column 5 line 65 – column 6 line 13).

Regarding claim 3, Saeki discloses wherein the parallel branch are formed from identical groups of series-connected battery elements which are connected in series with respective controlled switch (figure 3 items E_{1-2}; column 4 lines 52 – 55).

Regarding claim 10, Saeki disclose wherein the state monitoring means comprise a respective microprocessor per parallel branch for the purpose of controlling the respective switch (figure 7 item 2-1 – 2-3; column 10 lines 6 – 15: item 2 is an integrated circuit, MM1309, see attached 892).

Regarding claim 17, Saeki discloses wherein the discharge control circuit for a battery pack comprising:

a rechargeable battery elements which are arranged in respective parallel branches of a parallel circuit of battery voltage sources (figure 3 items E_{1-2}), the discharge control circuit comprising state monitoring means and switches (figure 3 items 2 and 5-8), which can be controlled by the state monitoring means for interrupting the current flow or releasing the current flow, each parallel branch

having in series with the battery voltage source comprising one or more battery elements represented by it, a respective controllable switch having an integrated diode or one which is connected in parallel therewith, which is conductive in the discharge current flow direction, characterized in that the state monitoring means are set so as to switch the respective controllable switch from a high resistance state to a low-resistance state when a discharge current having a minimum current level flows through the diode (column 9 line 21 – column 10 line 5: controllable switches items 6 and 8 turn off when a high level signal is applied to the switches and the same switches are turned on when a low level switch is applied. This can be understood to be switching from a high resistance state to a low resistance state because, as disclosed in column 10 lines 1 – 10, high resistance elements separate the battery cells, which provide the high resistance to be switched to a low resistance).

Regarding claim 12, Saeki discloses wherein the controllable switches are transistor, in particular field-effect transistors (figure 3 items 5 – 8 disclose FETs).

Regarding claim 13, Saeki discloses wherein the state monitoring means comprise at least one microprocessor preferably at least in each case one microprocessor for each parallel branch (column 10 lines 6 – 15: an integrated circuit, MM1309 is a microprocessor, see attached 892; figure 7 item 2-1 – 2-3 are connected to each parallel battery branch).

Regarding claim 14, Saeki discloses wherein a battery control circuit combined therewith, wherein the discharge control circuit comprising state monitoring

means (figure 3 item 2) and switches which can be controlled by the state monitoring means for interrupting the current flow or releasing the current flow (figure 3 items 5 – 8), each parallel branch having in series with the battery voltage source comprising one or more battery elements represented by it, a respective controllable switch having an integrated diode, or one which is connected in parallel therewith, which is conductive in the discharge current flow direction (figure 3 items 5 and 6 have diodes connected in parallel), characterized in that the state monitoring means are set so as to switch the respective controllable switch from a high-resistance state to a low resistance state when a discharge current having a minimum current level flows through the diode (column 9 line 21 – column 10 line 5: controllable switches items 6 and 8 turn off when a high level signal is applied to the switches and the same switches are turned on when a low level switch is applied. This can be understood to be switching from a high resistance state to a low resistance state because, as disclosed in column 10 lines 1 – 10, high resistance elements separate the battery cells, which provide the high resistance to be switched to a low resistance).

Regarding claims 15 and 18, Saeki discloses wherein the charge control circuit as claimed in one of the claims 1-10 and the discharge control circuit as claimed in 11 – 13 combined therewith (column 5 line 65 – column 6 line 13: charging and discharging circuits are comprised within the same system).

Regarding claim 19, Saeki discloses wherein a battery pack having the charge control circuit integrated therein and also having integrated therein a discharge control circuit which comprises state monitoring means (column 10 lines 6 – 15: an integrated circuit, MM1309 is a microprocessor, see attached 892; figure 7 item 2-1 – 2-3 are connected to each parallel battery branch; column 5 line 65 – column 6 line 13: charging and discharging circuits are comprised within the same system) and switches (figure 3 items 5 – 8 disclose FETs), which can be controlled by the state monitoring means for interrupting current flow or releasing the current flow (column 5 line 65 – column 6 line 13), each parallel branch having, in series with the battery voltage source comprising one or more battery elements represented by it, a respective controllable switch having an integrated diode (figure 3 items 5 and 6 show integrated diode with switch), or one which is connected in parallel therewith, which is conductive in the discharge current flow direction, characterized in that the state monitoring means are set so as to switch the respective controllable switch from a high resistance state to a low-resistance state when a discharge current having a minimum current level flows through the diode (column 9 line 21 – column 10 line 5: controllable switches items 6 and 8 turn off when a high level signal is applied to the switches and the same switches are turned on when a low level switch is applied. This can be understood to be switching from a high resistance state to a low resistance state because, as disclosed in column 10 lines 1 – 10, high resistance elements separate the

battery cells, which provide the high resistance to be switched to a low resistance).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 4 – 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saeki (U.S. 6,051,955) in view of Rahman (U.S. 5,990,664).

Regarding claim 4, Saeki does not disclose the invention as claimed. Rahman discloses in column 4 lines 7 – 53 wherein the temperature is monitored by a temperature sensor within the microcontroller, item 30. At the time of invention, it would have been obvious to a person of ordinary skill in the art to modify the Saeki system with the Rahman system so that the battery's temperature is monitored and protected from overheating.

Regarding claims 5, and 7 – 9, Saeki does not disclose the invention as claimed. Rahman discloses in column 4 lines 7 – 53 protection switches, items SW1 and SW2 are used to control the circuitry in reference to the temperature, current and time. At the time of invention, it would have been obvious to a person of ordinary skill in the art to modify the Saeki system with the Rahman

system so that the battery's temperature is monitored and protected from overheating and overcharging.

Regarding claim 6, Saeki does not disclose the invention as claimed. Rahman discloses in column 4 lines 7 – 53 wherein the current is monitored by the microcontroller, item 30. At the time of invention, it would have been obvious to a person of ordinary skill in the art to modify the Saeki system with the Rahman system so that the battery does not become damaged from overcharge.

Response to Arguments

5. Applicant's arguments filed 3/16/07 have been fully considered but they are not persuasive. **Regarding claims 16 and 17,** the applicant argues wherein the complete battery pack is not disconnected because one single batter cell assumes a state causing the state monitoring means. Saeki discloses in column 5 line 65 – column 6 line 14 wherein the FETs are turned off to selectively interrupt or release only one respective parallel branch. The complete battery pack is disconnected as the FETs are turned off. The applicant continues to argue wherein the Rahman reference does not describe the battery protection circuits. Rahman discloses in figure 3 item 18 wherein a protection circuit is used to protect the batteries.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexis Boateng whose telephone number is (571) 272-5979. The examiner can normally be reached on 8:30 am - 6:00 pm, Monday - Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Karl Easthom can be reached on (571) 272-1989. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AB

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SUPERVISORY PATENT EXAMINER